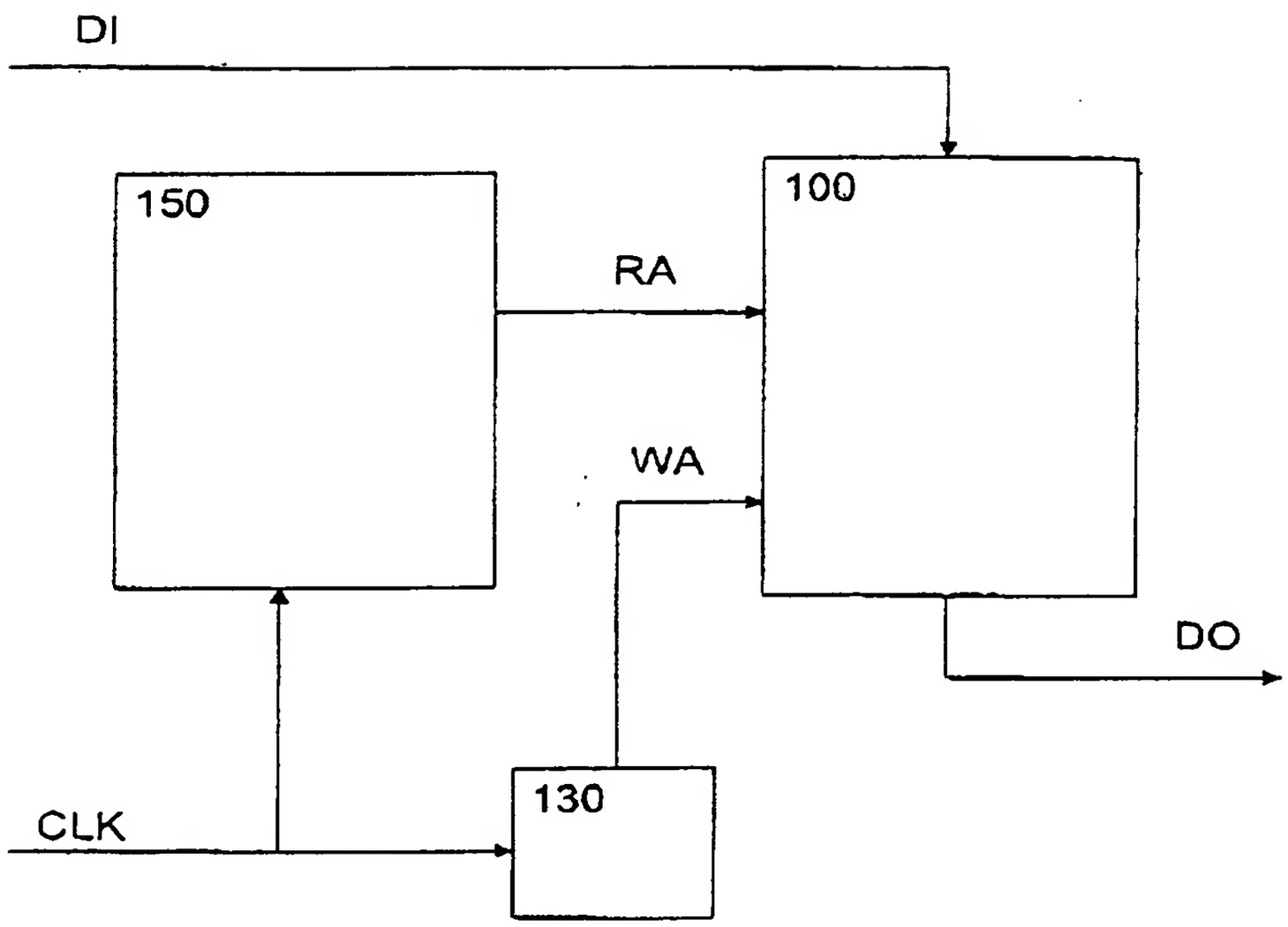

Fig. 1

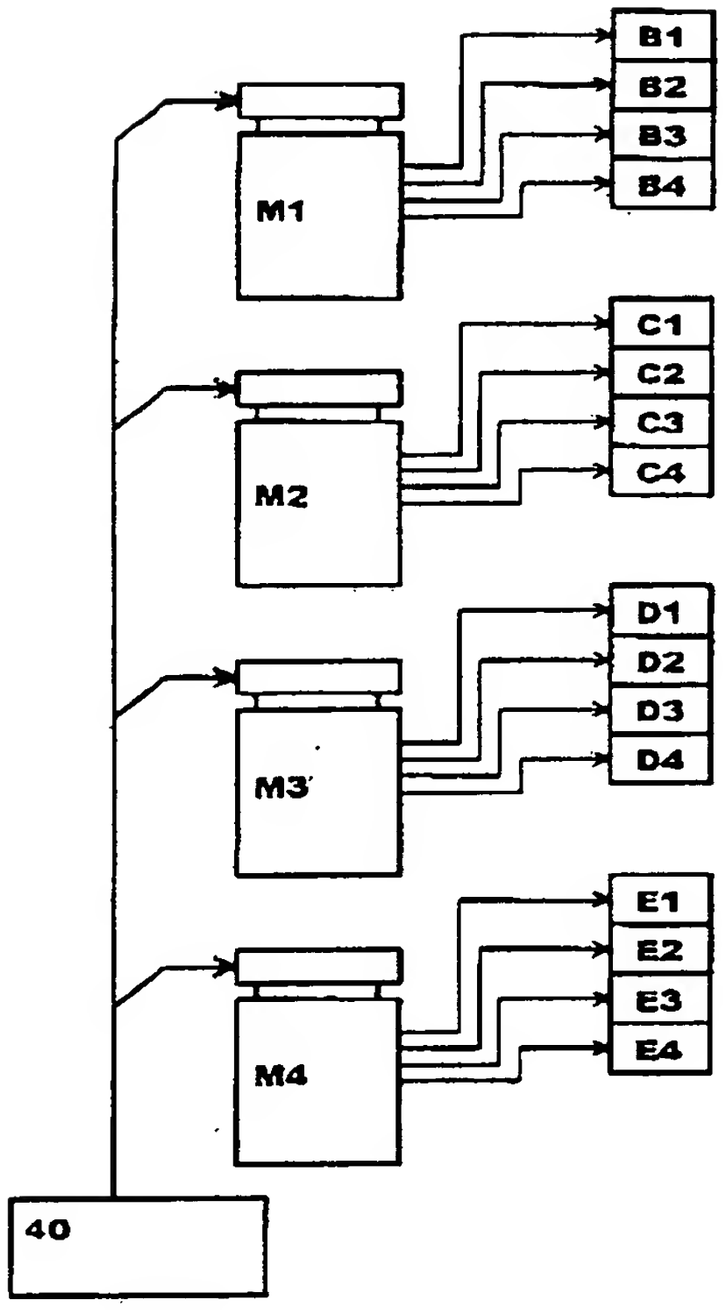

Fig. 2

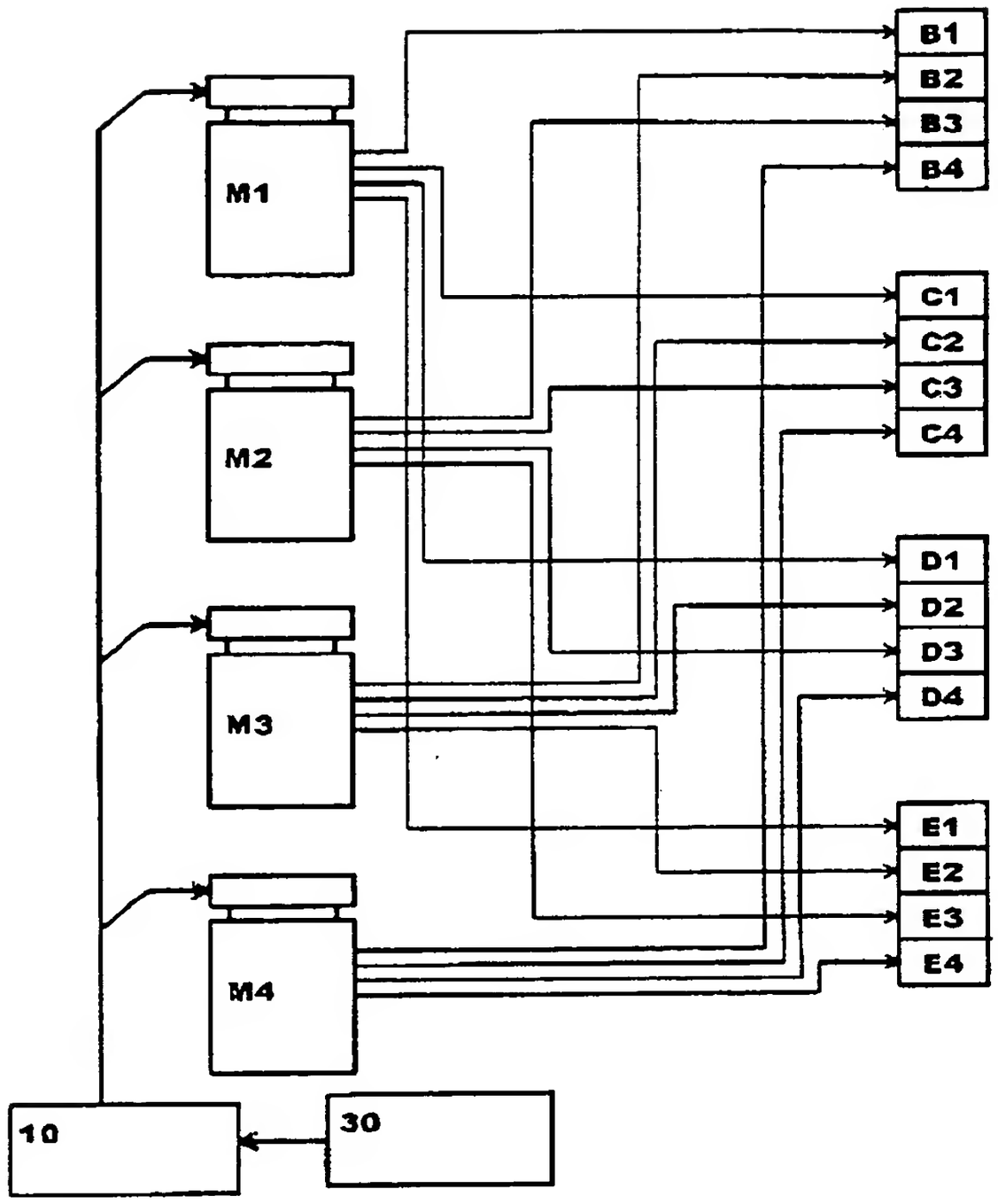

Fig. 3

Block	Clock Cycle	Symbol Access Scheme				RAM Access Scheme			
		Original		Modified		Linear		Interleaved	
		Linear	Interl.	Linear	Interl.	RAM	Addr	RAM	Addr
1	1	0	933	0	933	1	0	1	933
	2	1	2833	1	2981	1	1	3	933
	3	2	1883	2	1957	1	2	2	933
	4	3	3783	3	4005	1	3	4	933
2	1	950	313	1024	313	2	0	1	313
	2	951	2213	1025	2361	2	1	3	313
	3	952	1263	1026	1337	2	2	2	313
	4	953	3163	1027	3385	2	3	4	313
3	1	1900	764	2048	764	3	0	1	764
	2	1901	2664	2049	2812	3	1	3	764
	3	1902	1714	2050	1788	3	2	2	764
	4	1903	3614	2051	3836	3	3	4	764
4	1	2850	65	3072	65	4	0	1	65
	2	2851	1965	3073	2113	4	1	3	65
	3	2852	1015	3074	1089	4	2	2	65
	4	2853	2915	3075	3137	4	3	4	65

Fig. 4

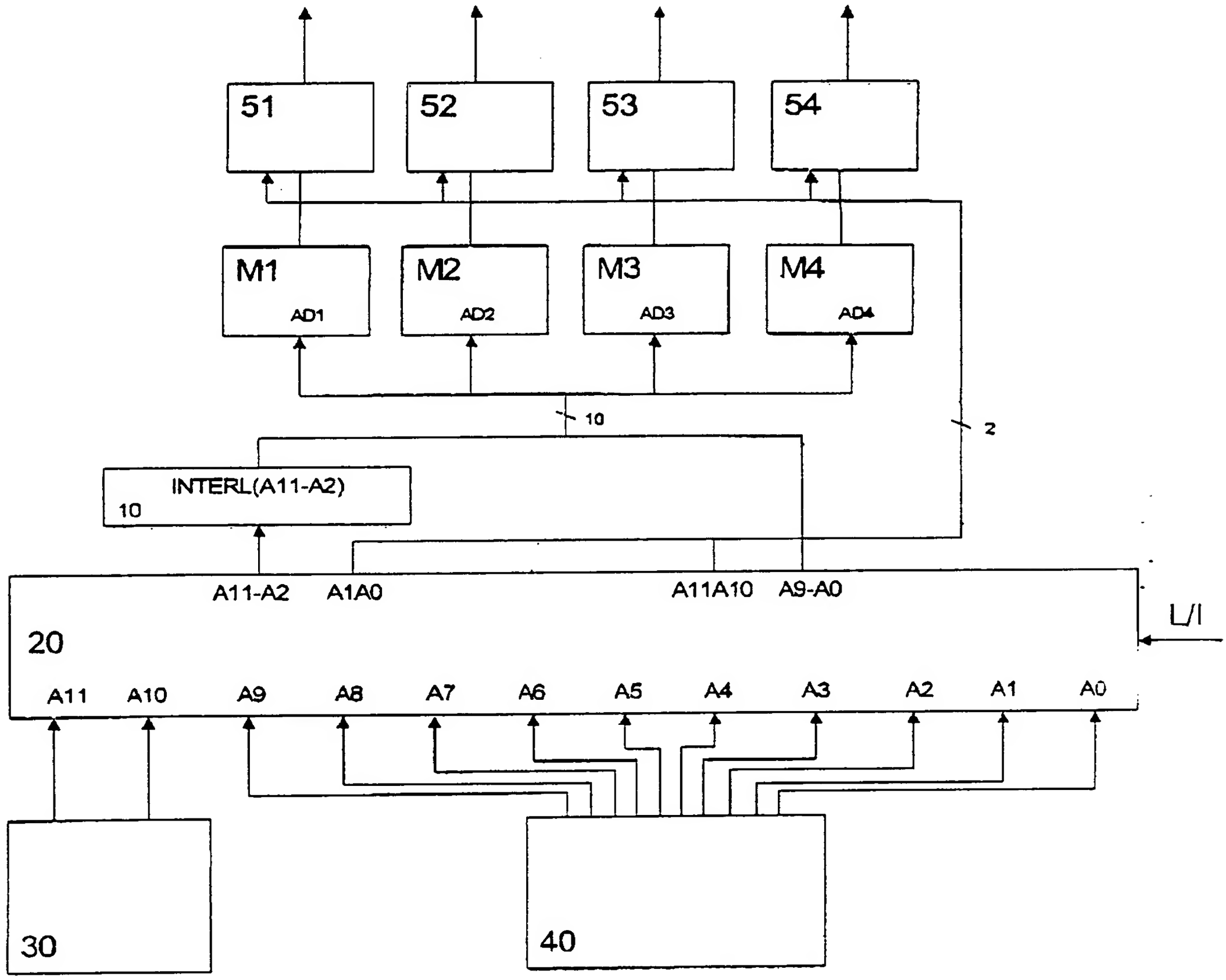
51
52
53
54
M1
AD1
M2
AD2
M3
AD3
M4
AD4
10
2
INTERL(A11-A2)
10
A11-A2
A1A0
A11A10
A9-A0
L/I
20
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
30
40

Fig. 5